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Three Phase Power Factor Correction Using SEPIC In DCM With Isolation

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Abstract

The improvement of power quality are required in AC-DC converters in terms of power factor correction. The PF is improved by reduction of total harmonic distortion at input of ac supply. Also high PF needed precisely regulated dc output. This paper briefly explains a three phase rectifer with high PF using single-ended primary-inductance converter (SEPIC) operating in discontinuous conduction mode with the analysis and design. The high PF at the input ac mains is attained through the use of current control loop. Average current mode control is used in proposed topology. The DCM topology is implemented for attain improved power factor in an effective and simple manner. The advantages of DCM operation are turn-on of the power switches at zero-current, turn-off the output diode at zero-current and simple control circuitry.

Keywords: Discontinuous conduction mode (DCM), power factor correction (PFC), single-ended primary-inductor converter (SEPIC),Single stage PFC

Introduction

In current cenaro, the use of ac to dc converters are widely increased. The ac to dc converters used in uninterrupted power supplies (UPSs), many offline power supplies such as adjustable-speed drives, battery energy storage and switch-mode power supplies. In an ac/dc converter it contains a diode-bridge rectifier, a bulky capacitor and a dc/dc converter which produces input current with high distortion, which causes a large amount of harmonics and a low power factor (PF).

Harmonics are the non-linearity of the input impedance. The input voltage varies with the variation of input impedance, which results distortion of the input current and hence, this distortion will cause for low power factor. Power factor correction techniques are used to increase the PF by reducing the harmonic distortion. The addition of power factor correction circuits increase the efficiency of power usage of equipment used in industries and domestic applications.

The common power factor correction method is using DC-DC Boost converter, with the proper control, connected to a diode bridge for single-phase systems. For high and medium power applications, three-phase topologies are used. The most common power factor correction circuit in three phase systems is six-switch PWM boost converters. The main disadvantage of this topology is higher output voltage than peak value of input voltage. In the case of buck topologies the output voltage is smaller than input voltage and not applicable in high voltage variations. The above problems can be solved by using a buck- boost converter. But the output of the buck-boost converter has inverted polarity. The conventional power factor correction methods consists of three stage power processing. The drawback of three stage PFC circuit is the reduced overall efficiency.

The solution for all the problems with conventional PFC techniques is proposed in this paper. This paper deals with single stage three phase PFC using SEPIC. Also the proposed topology is operating in discontinues conduction mode.

Proposed system

The proposed topology is generated by combining three single phase SEPIC power factor correction circuits using isolation transformers. The fig. 1(a) shows a single phase SEPIC. The modification done in SEPIC with isolation transformer for power factor correction is shown in fig. 1(b). The main advantage of SEPIC converter over other topologies was it has step up/down capability and non-inverted regulated output voltage.

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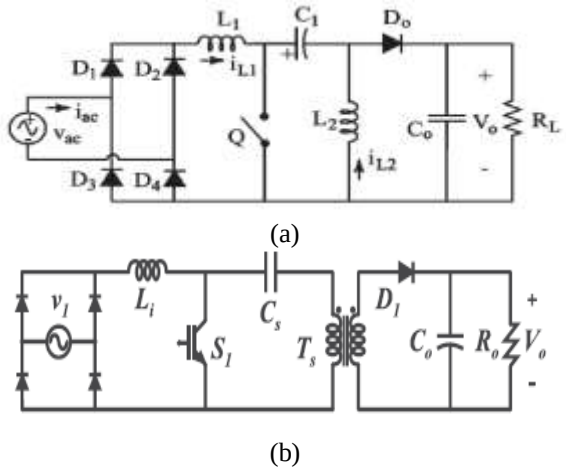


Fig. 1. Single phase (a) Conventional SEPIC (b) Modified SEPIC

Due to the output diode presented in the SEPIC the output capacitor has a high current peak. Due to higher output capacitance with low ESR maintain low ripple voltage on the output. The proposed topology is shown in fig. 2. The output of three single phase isolated converters connected in parallel. Average current mode control technique is adopted for the proposed system. Subheading should be 10pt Times new Roman, justified.

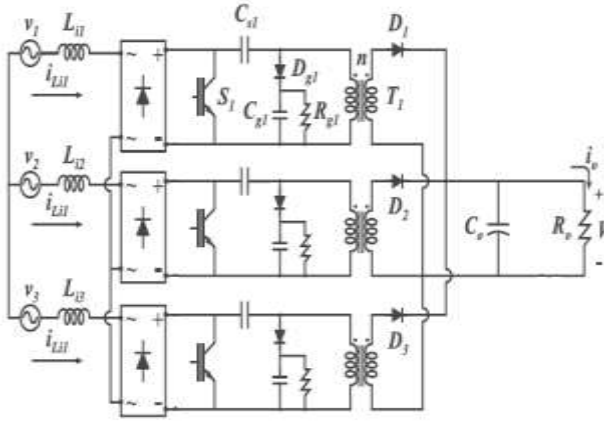


Fig. 2. Proposed system

Princple of operation

The DCM operation of a SEPIC converter defined using current through output diode is discontinuous when switch is in off state. Due to the DCM operation mode the converter can attain a sinusoidal input current which is in phase with input voltage. Thus simple control circuit is needed for the proposed power factor correction circuit. For the analysis purpose the proposed system is redraw as shown in fig. 3(a). The output voltage and output current relations shown in (1).

$$V_0=V_{01}=V_{02}=V_{03}$$
$$i_0=i_{01}+i_{02}+i_{03} \quad (1)$$

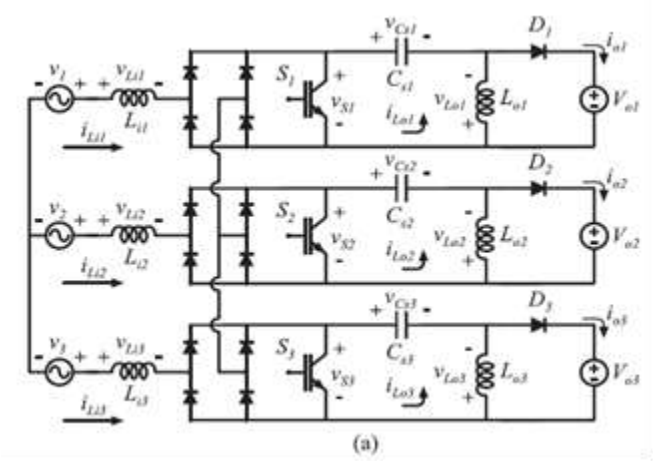
The fig. 4 shows the input voltage. To reduce the complexity of mathematical analysis one cycle is divided into equal sectors of 30^0 per sector which have similar behaviour in each sector. So explanation of one sector is needed. Consider the fourth sector to explain the working of proposed system. The relation of input voltages at the fourth sector is given by (2). The switches are operated simultaneously in proposed system.

$$V_1>V_2>V_3$$
$$V_1>0,\ V_2<0,\ V_3<0 \quad (2)$$

For proper working the input inductances must be higher than output inductances and SEPIC capacitor voltages are equal to input voltages, given in (3). Also relation (4) is valid due to constructive symmetry.

$$L_{i1}>L_{o1},\ L_{i2}>L_{o2},\ L_{i3}>L_{o3}$$
$$V_{cs1}=|V_1|,\ V_{cs2}=|V_2|,\ V_{cs3}=|V3| \quad (3)$$

$$L_{i1}=L_{i2}=L_{i3}=L_i$$
$$L_{o1}=L_{o2}=L_{o3}=L_o$$
$$C_{s1}=C_{s2}=C_{s3}=C_s \quad (4)$$



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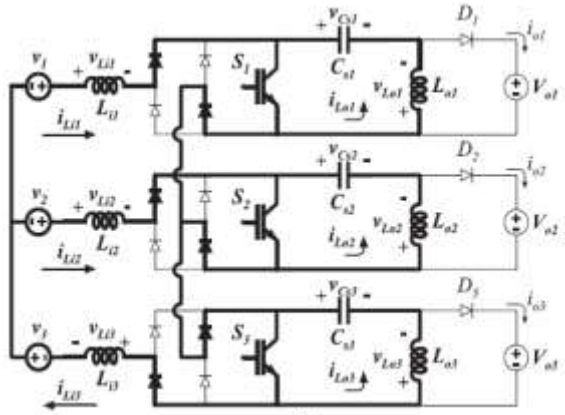
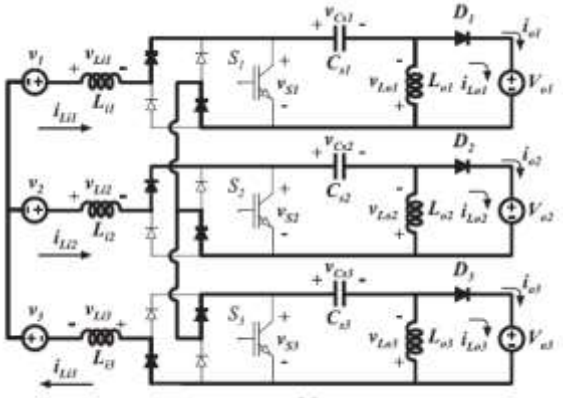
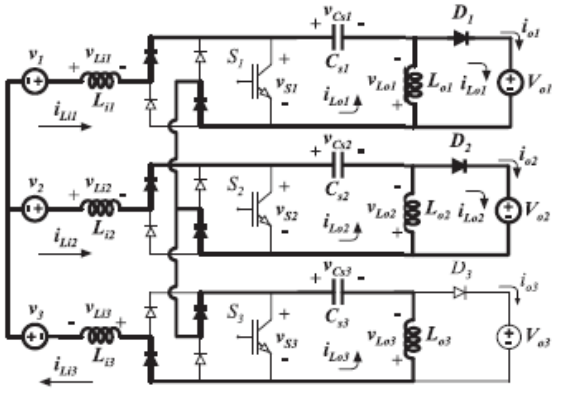


(b)

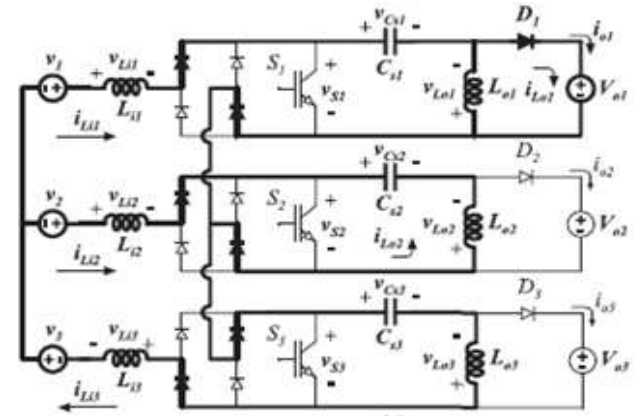


(c)

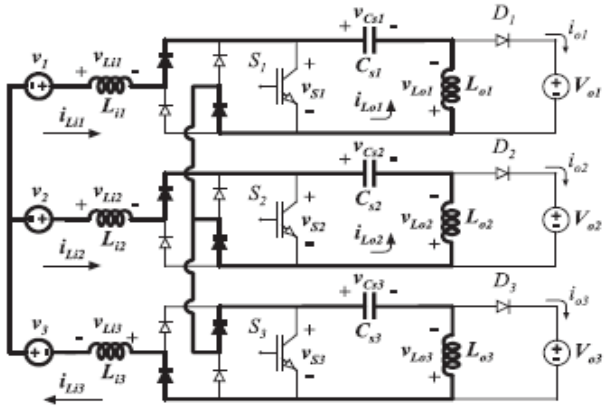


(d)

In the beginning of first stage the three switches are conducting. The output diodes are reverse biased and the input inductor stores the energy. And the energy transferred to output inductors through SEPIC capacitors. The first stage shows in fig. 3(b). When switches are turned off, the second stage starts. The second stage shows in fig. 3(c). In the second stage the stored energy in the output inductor transferred into system output



(e)



(f)

Fig. 3. Operating stages

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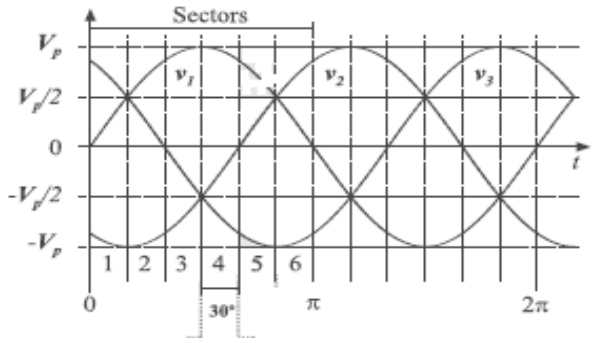

Fig. 4.Input voltage

The input voltage level at the sector four is different. So the energy store level is also different. From the wave form for the sector four, the voltage V_3 is lowest. So the output diode D_3 is first blocked. That is the third stage, shown in fig. 3(d).At the same time the input and output inductor values are same for third phase (L_{i3}=L_{o3}). The fourth stage starts when next diode is lowest voltage diode is blocked. In the fourth sector V_2 is the second lowest voltage. So the diode D_2 is

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blocked and shown in fig. 3(e). In the fifth stage all the three output diodes are blocked and shown in fig. 3(f). At that time no power is transferred to the system output. Thus, the proposed system is said to be in DCM operating mode.

From the operation mode description the inductor and output diode currents in each stage shows in fig. 5. The average output current value is given by (5).

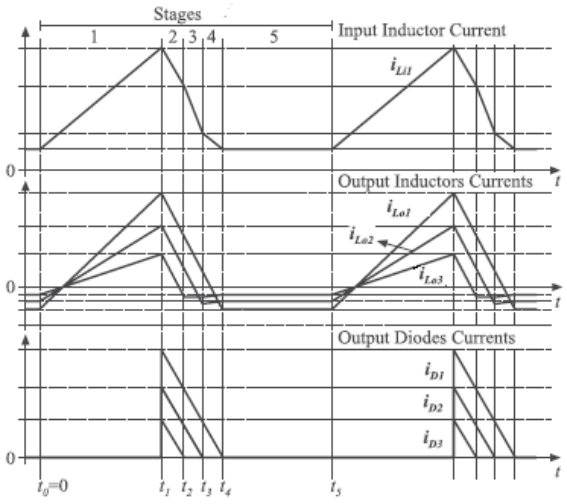

Fig. 5. Inductor currents and output diode currents

$$I_0 = \frac{3}{4}\frac{V_p^2 D^2}{V_0 f_s L_{eq}} \qquad (5)$$

Where,

$$L_{eq} = \frac{L_i L_o}{L_i + L_o} \qquad (6)$$

The average output voltage is given by (8) and the duty cycle limit is given by (9). The input and output power is given by (10).

$$V_o = V_p D\sqrt{\left(\frac{3R_o}{4f_s L_{eq}}\right)} \qquad (8)$$

$$D_{lim} < \frac{G}{(1+G)} \qquad (9)$$

$$P_o = P_i = P_{3\emptyset} = \frac{3}{2}V_p I_0 = \frac{3}{4}\frac{V_p^2 D^2}{f_s L_{eq}} \qquad (10)$$

Simulation results

Simulation is done in MATLAB. The control technique used is average current mode control. In average current control method the switching frequency is fixed, noise immunity is excellent, speed of the response is fastest and ripple current is fixed

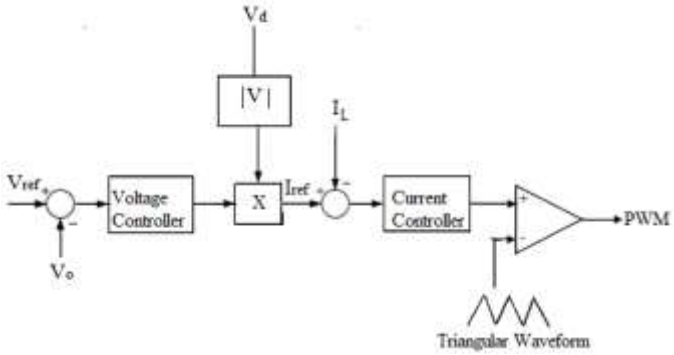

Fig. 6 Average current mode control

The specifications for power supply is given in table 1 and designed circuit parameter values are given in table 2.

Table 1. Power supply specifications

Parameters	Value
Input phase voltage	230 V
Supply frequency	50Hz
Output DC voltage	400 V
Rated power	1kW
Output current	2.5 A
Input current	5 A

The simulation results shown in table 3. The input current and voltage waveforms shown in fig. 7. It shows that the input currents and input voltages are in phase and sinusoidal. The output current and voltage waveforms shown in fig. 8.

Table 1. Designed Circuit Parameters

Parameters	Value
Switching frequency	40kHz
Designed duty cycle	.6349
Input inductance	22.22 mH
Output inductance	365.273µH
Switching capacitance	11.9µF
Output capacitance	2000 µF

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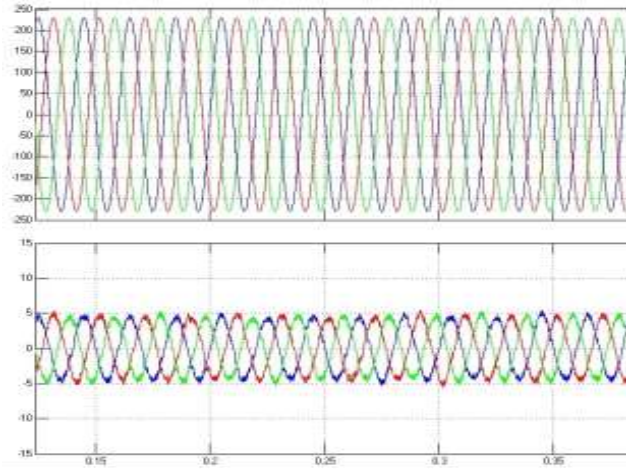

Fig.7 Input voltage and current waveform

It shows that the input currents and input voltages are in phase and sinusoidal. The output diode current and output currents shows in fig. 8. The waveforms are shows that the PF of proposed topology is increased.

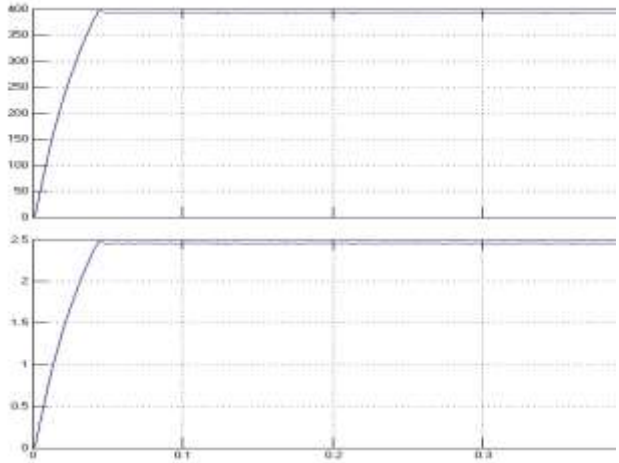

Fig. 8 Output voltage and current waveform

Table 3. Simulation Results

Parameters	Value
Input phase voltage	230 V
Input current	4.8 A
Input P.F.	0.9999
Output current	2.455 A
Output DC voltage	393 V
Output power	964.815W

The output diode current and output currents shows in fig. 9. The results are shows that the PF of proposed topology is very close to unity.

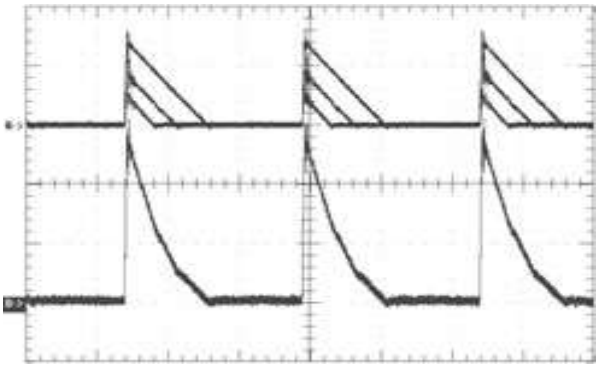

Fig. 9 Output Output diode current

Conclusion

This paper deals with a three-phase single stage high PF rectifier topology based on the dc–dc SEPIC operating in DCM. Theoretical analysis was detailed in this paper. The simulation of proposed topology gives that by using this topology, the power factor of the three phase rectifier circuits were increased and it is very close to unity.

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